

DEVELOPMENT DATA

This data sheet contains advance information and specifications are subject to change without notice.



SAA7320

STEREO CMOS DAC FOR COMPACT DISC DIGITAL AUDIO SYSTEMS

GENERAL DESCRIPTION

The SAA7320 (DAC3) is a complete monolithic stereo CMOS 16-bit input digital-to-analogue converter designed for application in low/mid-cost portable compact disc systems.

Features

- I²S data input
- 3-stage digital filter incorporating F.I.R. filter, linear interpolator and sample and hold
- 2nd order noise shaper to provide a signal-to-noise ratio of > 90 dB
- 16-bit resolution from a 1-bit converter, using switched capacitor integrator
- 3rd order low-pass filter to reduce out-of-band noise
- -12 dB attenuation, de-emphasis and mute control
- Low power consumption (typ. 300 mW)
- Single supply operation (+ 5 V)
- -40 to + 85 °C operating temperature range

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage (analogue)		V _{DDA}	4,5	5,0	5,5	V
Supply current (analogue)		I _{DDA}	—	20	*	mA
Supply voltage (digital)		V _{DD}	4,5	5,0	5,5	V
Supply current (digital)		I _{DD}	—	40	*	mA
Signal-to-noise ratio at the analogue outputs	0 dB input	S/N	—	90	—	dB
Input voltage ranges WSI, CLI, DAI, DEC, ATT						
Input voltage LOW	note 6	V _{IL}	0	—	+ 0,8	V
Input voltage HIGH	note 6	V _{IH}	2,0	—	V _{DD} + 0,5	V
Output voltage ranges WSO, CLO, DAO, XSYS,						
Output voltage LOW	note 6	V _{OL}	0	—	+ 0,4	V
Output voltage HIGH	note 6	V _{OH}	2,4	—	V _{DD} + 0,5	V
Operating frequency XTAL		f _{XTAL}	8,0	11,2896	12,3	MHz
Operating ambient temperature range		T _{amb}	-40	—	+ 85	°C

* Value to be fixed.

For explanation of notes see "Notes to the characteristics".

PACKAGE OUTLINE

SAA7320GP: 44-lead QFP; plastic (SOT205A).

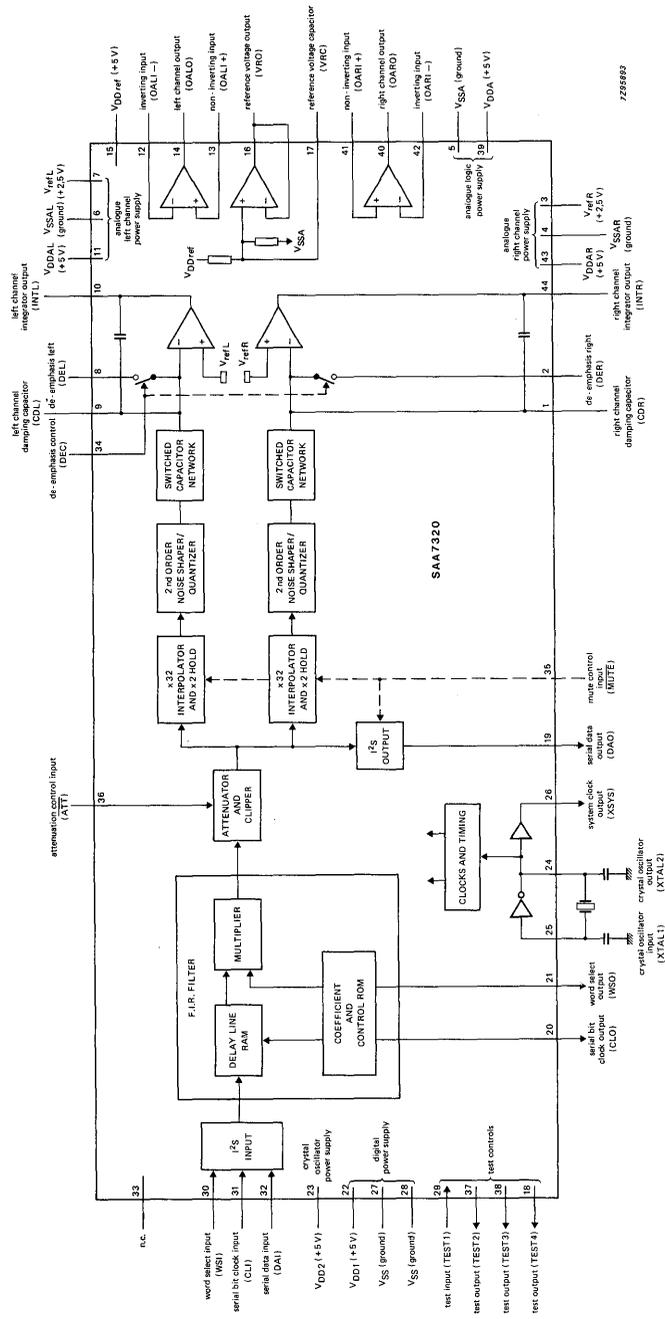


Fig. 1 Block diagram.

PINNING

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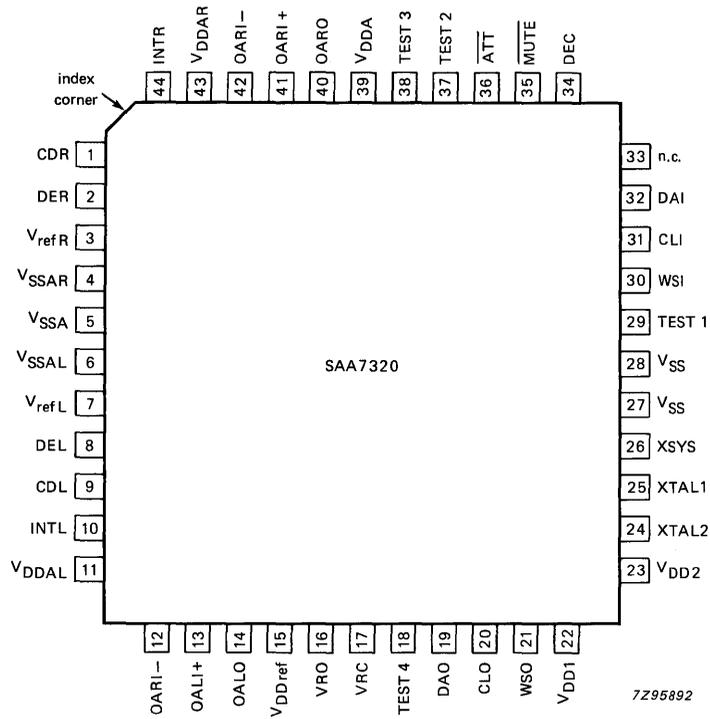


Fig. 2 Pinning diagram.

Pin functions

pin no.	mnemonic	description
1	CDR	Capacitor Damping Right: damping capacitor for the right channel switched-capacitor integrator.
2	DER	De-emphasis Right: connection to the de-emphasis switch in the feedback of the right channel integrator.
3	V _{refR}	Reference voltage Right: reference voltage input for the analogue right channel ground (+ 2,5 V typ.).
4	VSSAR	Ground: ground connection for the analogue right channel.
5	VSSA	Ground: ground connection for logic in the analogue section.
6	VSSAL	Ground: ground connection for the analogue left channel.
7	V _{refL}	Reference voltage Left: reference voltage input for the analogue left channel ground (+ 2,5 V typ.).
8	DEL	De-emphasis Left: connection to the de-emphasis switch in the feedback of the left channel integrator.
9	CDL	Capacitor Damping Left: damping capacitor for the left channel switched-capacitor integrator.
10	INTL	Integrator Left: output from the left channel switched-capacitor integrator.
11	VDDAL	Power Supply: + 5 V supply voltage for the analogue left channel.
12	OALI-	Operational Amplifier Left Input -: inverting input to the left channel low-pass filter operational amplifier.
13	OALI+	Operational Amplifier Left Input +: non-inverting input to the left channel low-pass filter operational amplifier.
14	OALO	Operational Amplifier Left Output: output from the left channel operational amplifier.
15	VDDref	Power Supply: +5 V supply voltage for the reference voltage generator.
16	VRO	Reference Voltage Output: internal reference voltage output (+ 2,5 V typ.).
17	VRC	Reference Voltage Capacitor: internal reference voltage high impedance node requiring an external smoothing capacitor.
18	TEST4	Test output 4: pin should be left open-circuit.
19	DAO	I²S Serial Data Output: is a 16-bit linear two's-complement PCM signal at a data rate of 176,4 kHz (typ.) formatted in accordance with I ² S. After 4 x upsampling by the digital filter this signal is output so that an external DAC could be used; combined with CLO and WSO it can be considered as a master transmitter.
20	CLO	I²S Serial bit Clock Output: f _{CLO} = 5,6448 MHz typ.
21	WSO	I²S Word Select Output: 176,4 kHz typ.
22	VDD1	Power supply: + 5 V supply voltage for the digital section.
23	VDD2	Power Supply: + 5 V supply voltage for the crystal oscillator.
24	XTAL2	Crystal oscillator output: drive output to clock crystal.
25	XTAL1	Crystal oscillator input: input from crystal oscillator or external clock input (11,2896 MHz typ.).
26	XSYS	System clock output: buffered output from crystal oscillator
27, 28	VSS	Ground: ground connection for the digital section.

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pin no.	mnemonic	description
29	TEST1	Test input 1: pin should be connected to ground.
30	WSI	I²S Word Select Input: 44,1 kHz typ. WSI together with CLI, is used to clock the I ² S serial data input (DAI) and synchronize the main timing chain.
31	CLI	I²S Serial bit Clock Input: $f_{CLI} = 2,8224 \text{ MHz typ.}$
32	DAI	I²S Serial Data Input: is a 16-bit linear two's-complement PCM signal formatted in accordance with I ² S. If more than 16 bits are supplied then the least significant bits (LSBs) will be truncated.
33	n.c.	not connected.
34	DEC	De-emphasis Control: this input switches an extra external capacitor network into both the analogue left and right channel integrator feedback.
35	$\overline{\text{MUTE}}$	Mute: when active LOW this Schmitt trigger control input will force the interpolator data input to zero. It will also force the I ² S data output (DAO) to zero.
36	$\overline{\text{ATT}}$	Attenuation: when active LOW this control input provides -12 dB attenuation to the analogue output amplitude.
37	TEST2	Test output 2: pin should be left open-circuit.
38	TEST 3	Test output 3: pin should be left open-circuit.
39	VDDA	Power Supply: + 5 V supply voltage for logic in the analogue section.
40	OARO	Operational Amplifier Right Output: output from the right channel operational amplifier.
41	OARI+	Operational Amplifier Right Input +: non-inverting input to the right channel low-pass filter operational amplifier.
42	OARI-	Operational Amplifier Right Input -: inverting input to the right channel low-pass filter operational amplifier.
43	VDDAR	Power Supply: + 5 V supply voltage for the analogue right channel.
44	INTR	Integrator Right: output from the right channel switched-capacitor integrator.

FUNCTIONAL DESCRIPTION

General

The SAA7320 CMOS DAC heavily oversamples to several MHz (256 x the sampling frequency, f_s), so that the band-limiting filters required for waveform smoothing and out-of-band noise reduction are mainly digital. In addition to the digital filters the circuit contains active components for analogue post filtering. In most applications very few external components are required. An output after the 4 x upsampling filter allows the circuit to be used as an interface between the decoder and external DAC in high-performance compact disc systems. The SAA7320 requires only one +5 V supply; the required reference voltage is generated internally.

Separate supply pins for each of the 1-bit DACs achieves high performance signal-to-noise ratio and channel separation.

There is no phase delay between the two analogue outputs despite the fact that the upsampling filter structure is multiplexed between the two data channels.

Oversampling digital filter

This is a 3-stage digital filter.

- The first stage provides 4 x oversampling to 176,4 kHz using a 128-tap F.I.R. low pass filter. Data is stored in a cyclic RAM, the filter coefficients in a ROM and the convolutions are performed using an array multiplier.
- The second stage is a 32 x oversampling linear interpolator.
- The third stage provides 2 x upsampling using a sample and hold, giving a total of 256 x upsampling (11,2896 MHz).

The first stage oversamples to 176,4 kHz with a band-pass ripple of $\pm 0,035$ dB and a stop-band attenuation of -60 dB above 24,2 kHz. It also contains frequency response compensation for the interpolator/analogue post-filtering roll-off and coefficient scaling to prevent overflow in the noise shaper.

The characteristics of the F.I.R. filter are shown in Fig. 8.

Switched-capacitor DAC

The digital-to-analogue conversion is achieved with a 1-bit DAC oversampled to 256 f_s with second-order noise shaping performed digitally to give a 1-bit Pulse Density Modulated (PDM) code with a signal-to-noise ratio of > 90 dB. Integral with the actual 1-bit converter is a first-order low-pass filtering action which reduces the total HF noise power.

A switched capacitor technique is used for the 1-bit DAC which converts the PDM stream to an analogue signal with a signal-to-noise ratio of > 90 dB. A fixed charge is either added or subtracted from the virtual earth node of a first-order filter. As this output is a continuous time output a highly symmetrical operational amplifier is used to give a low distortion figure. The output slew rate of this filter is chosen so that the operational amplifier always remains within its high gain linear region.

An internally generated out-of-band dither signal is used to suppress audible idling patterns in the noise shaper at low signal levels. This signal is injected digitally into the x 32 upsampling interpolator at a frequency 352 kHz and a level of -20 dB.

FUNCTIONAL DESCRIPTION (continued)**Attenuation**

Attenuation is controlled by the \overline{ATT} input at pin 36. This input will allow an attenuation of the analogue output amplitude by -12 dB during track search.

De-emphasis and low-pass filter

Extra on-chip analogue circuitry provides post filtering:

- Input DEC (pin 34) switches an extra external capacitor network into both the left and right channel analogue integrator feedback to control roll-off.
Output from the right channel switched-capacitor integrator (INTR) is available at pin 44. Output from the left channel switched-capacitor integrator (INTL) is available at pin 10.
- A low-pass filter, for further attenuation of out-of-band noise, can be constructed using the internal CMOS operational amplifiers. The digital filter contains compensation for a third-order Butterworth filter with a -3 dB cut-off at 60 kHz.

I²S serial interface

The SAA7320 has two I²S ports incorporated; DAI (pin 32) and DAO (pin 19).

- DAI receives data from the Compact Disc decoder IC (or any 16-bit 44,1 kHz I²S source).
- DAO transmits the 4 x oversampled data to an external DAC.

The 'slave' receiver requires a serial bit clock input (CLI; pin 31) and a word select input (WSI; pin 30). To ensure that the filter is 'in-phase' with the input, the main timing chain is automatically synchronized to the incoming word select signal. The frequency of the data must also be synchronized to the filter by:

- the source supplying the 11,2896 MHz system clock via crystal oscillator input (XTAL1; pin 25).
or
- SAA7320 supplying the system clock to the source via XSYS (pin 26).

The SAA7320 will use only the 16 most significant bits of input data even though the I²S format allows a variable word length (see Fig. 4).

The 'master' transmitter supplies bit clock, word select and data signals at twice the frequency of the receiver to allow for the 4 x upsampling. Therefore all 16 bit positions are used.

Conversion path

The SAA7320 data conversion path is shown in Fig. 3. As both paths are identical only one path is shown. The data flow is in a serial format up to the linear interpolator stage and then separated into two channels.

CD3A application

A system application diagram of the CD3A with the DAC3 is shown in Fig. 9.



Purchase of Philips I²S components conveys a license under the Philips' I²S patent to use the components in the I²S-system provided the system conforms to the I²S specification defined by Philips.

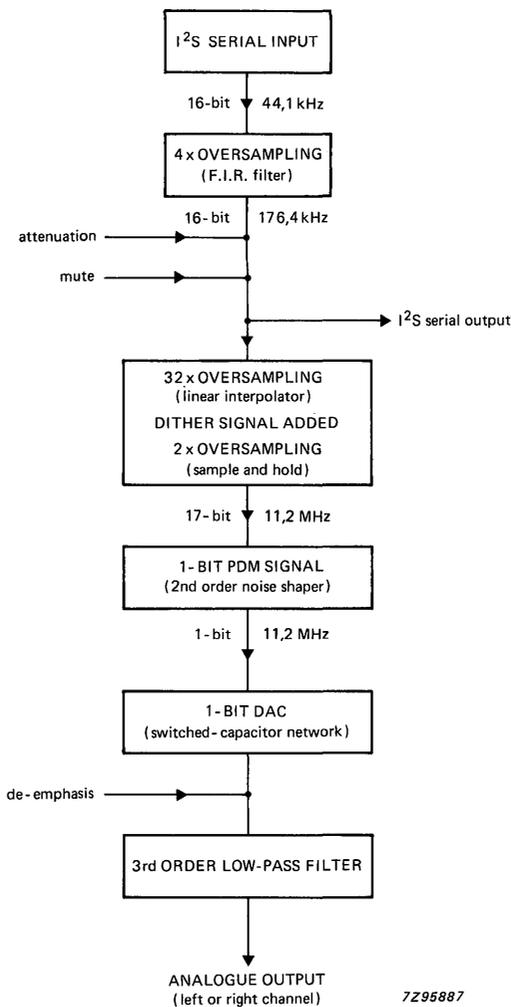


Fig. 3 Flow diagram of SAA7320 data conversion path (one channel).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage*	V_{DDA}	-0,5	+ 6,5	V
DC input voltage	V_I	-0,5	$V_{DD} + 0,5$	V
DC input diode current	I_{IK}	-	± 20	mA
DC output voltage	V_O	-0,5	$V_{DD} + 0,5$	V
DC output source or sink current	I_O	-	± 25	mA
DC V_{DD} or V_{SS} current (total)	I_{DD} or I_{SS}	-	$\pm 0,5$	A
Storage temperature range	T_{stg}	-65	+ 150	$^{\circ}C$
Operating ambient temperature range	T_{amb}	-40	+ 85	$^{\circ}C$
Electrostatic handling**	V_{es}	-1000	+ 1000	V

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* All V_{DD} and V_{SS} pins must be connected externally to the same power supply unit.** Equivalent to discharging a 100 pF capacitor through a 1,5 k Ω series resistor with a rise time of 15 ns.

CHARACTERISTICS

 $V_{DD} = 4,5 \text{ to } 5,5 \text{ V}; V_{SS} = 0 \text{ V}; T_{amb} = -40 \text{ to } +85 \text{ }^\circ\text{C}$ unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage (analogue)		V_{DDA}	4,5	5,0	5,5	V
Supply current (analogue)		I_{DDA}	—	20	*	mA
Supply voltage (digital)		V_{DD}	4,5	5,0	5,5	V
Supply current (digital)		I_{DD}	—	40	*	mA
ANALOGUE PART						
Reference voltage source						
VRO; VRC						
High impedance reference voltage level		V_{refC}	$0,45V_{DD}$	$0,5V_{DD}$	$0,55V_{DD}$	V
Output reference voltage relative to VRC		ΔV_{refO}	-10	0	+10	mV
Reference voltage output impedance		$ Z_{refO} $	—	2	4	Ω
Reference voltage inputs						
$V_{refL}; V_{refR}$	note 1					
Reference input voltage		V_{ref}	$0,45V_{DD}$	$0,5V_{DD}$	$0,55V_{DD}$	V
Outputs						
INTL; INTR						
Output level (RMS value)	note 2; $f_s = 44,1 \text{ kHz}$	$V_{AO(rms)}$	—	—	1,0	V
Output dynamic impedance		Z_{AO}	—	100	200	Ω
Output load resistance	to V_{ref}	R_L	10	—	—	$k\Omega$
Output load capacitance	to V_{ref}	C_L	—	—	+20	pF
Output DC level	to V_{ref}	V_{AODC}	-20	—	+20	mV

* Value to be fixed.

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parameter	conditions	symbol	min.	typ.	max.	unit
Filter characteristics	note 3					
Signal spectrum (0 dB = F.S.D. input)						
< 20 kHz		SS	-0,035	-	+ 0,035	dB
> 24,1 kHz		SS	-60	-	-	dB
Signal-to-noise ratio						
0 dB input		S/N	90	-	-	dB
-10 dB input		S/N	83	-	-	dB
Total harmonic distortion	at 0 dB/1 kHz	THD	-	-	-90	dB
Digital silence	Mute LOW		*	-96	-	dB
Channel separation	at 1 kHz	α	*	80	-	dB
Power supply rejection ratio to V_{DD}		PSRR	*	60	-	dB
Operational amplifiers						
Open loop gain		G_{ol}	*	85	*	dB
Output impedance		$ Z_O $	-	100	150	Ω
Input offset voltage		V_{Ios}	-10	-	+ 10	mV
Signal-to-noise ratio (20 Hz to 20 kHz)	note 4	S/N	+ 95	-	-	dB
Total harmonic distortion (20 Hz to 20 kHz)	note 5	THD	-	-	-94	dB
Unity gain bandwidth		G_{BW}	5	10	-	MHz
Output load to V_{ref} capacitive		C_L	-	-	200	pF
resistive		R_L	3	-	-	k Ω
DIGITAL PART						
Inputs						
WSI, CLI, DAI, DEC, <u>ATT</u>						
Input voltage LOW	note 6	V_{IL}	-0,5	-	+ 0,8	V
Input voltage HIGH	note 6	V_{IH}	2,0	-	$V_{DD} + 0,5$	V
Input leakage current	note 7	I_{LI}	-10	0	+ 10	μA
Input capacitance		C_I	-	-	10	pF

* Value to be fixed.

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
MUTE (Schmitt trigger)						
Switching voltage threshold						
rising		V_{thr}	$0,54V_{DD}$	$0,6V_{DD}$	$0,66V_{DD}$	V
falling		V_{thf}	$0,36V_{DD}$	$0,4V_{DD}$	$0,44V_{DD}$	V
Input leakage current	note 7	I_{LI}	-10	0	+ 10	μA
Input capacitance		C_I	-	-	10	pF
Crystal oscillator input						
External clock only XTAL1						
Input voltage LOW	note 6	V_{IL}	-0,5	-	1,5	V
Input voltage HIGH	note 6	V_{IH}	3,5	-	V_{DD} to 5 V	V
Input leakage current	note 7	I_{LI}	-10	0	+ 10	μA
Input capacitance		C_I	-	-	10	pF
Outputs						
DAO, CLO, WSO, XSYS						
Output voltage LOW	note 6; $-I_{OL} = 400 \mu A$	V_{OL}	-0,5	-	+ 0,4	V
Output voltage HIGH	note 6; $I_{OH} = 20 \mu A$	V_{OH}	2,4	-	$V_{DD} + 0,5$	V
Load capacitance		C_L	-	-	35	pF
Crystal oscillator						
see Fig. 7						
Input XTAL1						
Output XTAL2						
Operating frequency XTAL		f_{XTAL}	8,0	11,2896	12,3	MHz
Mutual conductance	100 kHz	G_m	1,5	-	-	mA/V
Small signal voltage gain	$G_v = G_m \times R_O$	G_v	3,5	-	-	V/V
Input capacitance		C_I	-	-	10	pF
Feedback capacitance		C_{FB}	-	-	5	pF
Output capacitance		C_O	-	-	10	pF
Input leakage current	note 7	I_{LI}	-10	-	+ 10	μA

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parameter	conditions	symbol	min.	typ.	max.	unit
TIMING						
External clock input						
XTAL1						
Input frequency ($f_s \times 256$)		f_c	8,0	11,2896	12,3	MHz
Input rise time	note 8	t_r	—	—	20	ns
Input fall time	note 8	t_f	—	—	20	ns
Input HIGH time (relative to clock period)	at 1,5 V	t_{HIGH}	45	—	55	%
System clock output						
XSYS						
Output rise time	note 9					
Output fall time	note 8	t_r	—	—	20	ns
Output HIGH time (relative to clock period)	note 8	t_f	—	—	20	ns
Output HIGH time (relative to clock period)	at 1,5 V note 10	t_{HIGH}	45	—	55	%
I²S TIMING						
Receiver						
see Fig. 5						
Clock input CLI						
Input clock period		t_{CK}	320	354	1000	ns
Input HIGH time		t_{CKH}	112	—	—	ns
Input LOW time		t_{CKL}	112	—	—	ns
Data inputs WSI, DAI						
Data set-up time		$t_{SU}; DAT$	40	—	—	ns
Data hold time		$t_{HD}; DAT$	0	—	—	ns

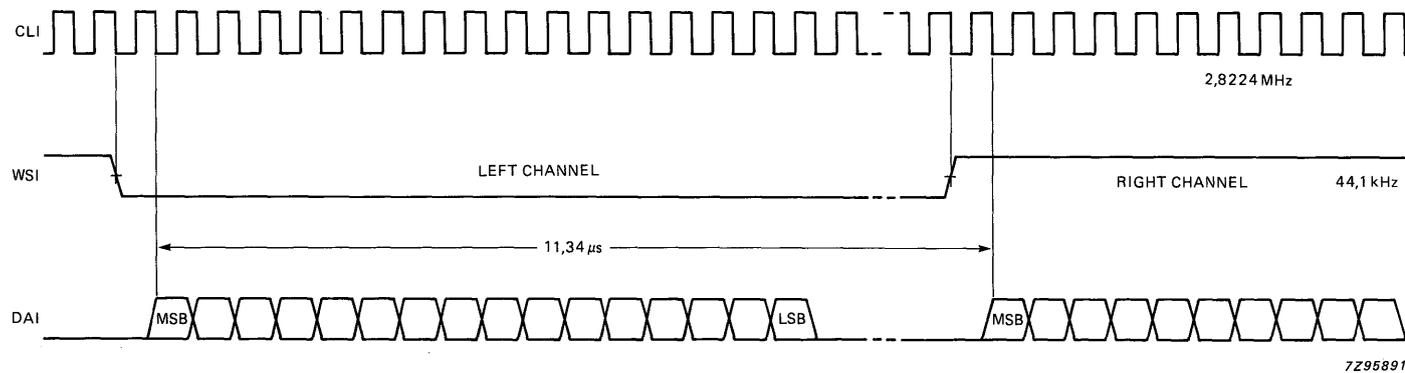
CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Transmitter	see Fig. 6					
Clock output CLO						
Output clock period		t _{CK}	—	2/f _C	—	ns
Output HIGH time		t _{CKH}	60	—	—	ns
Output LOW time		t _{CKL}	60	—	—	ns
Data WSO						
Data set-up time		t _{SU} ; DATWS	40	—	—	ns
Data hold time		t _{HD} ; DATWS	40	—	—	ns
Output rise time		t _r	—	—	20	ns
Output fall time		t _f	—	—	20	ns
Data output DAO						
Data set-up time		t _{SU} ; DATD	40	—	—	ns
Data hold time		t _{HD} ; DATD	40	—	—	ns
Output rise time		t _r	—	—	20	ns
Output fall time		t _f	—	—	20	ns

Notes to the characteristics

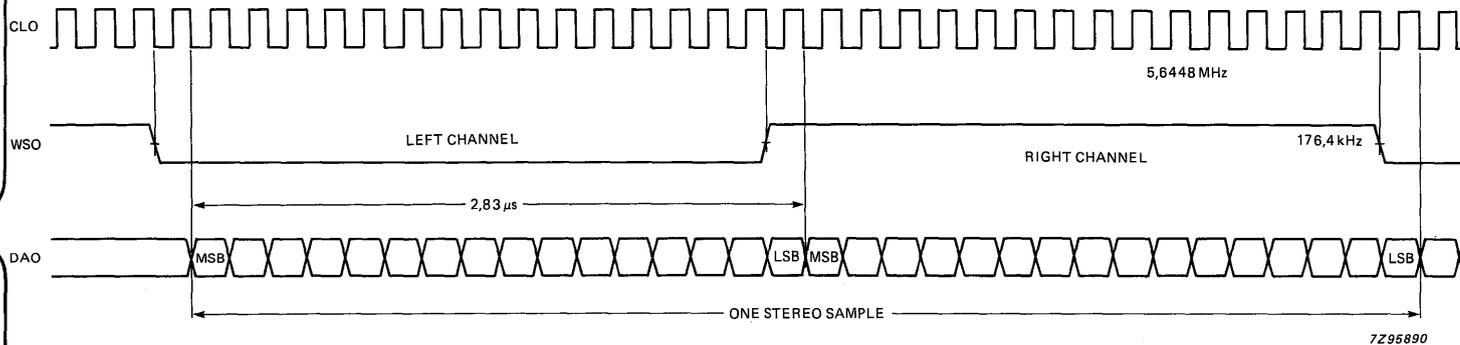
- Any noise at these inputs is transferred directly to the analogue outputs.
- Output levels depend on integrator components. Value shown is for maximum digital code.
- The filter characteristics apply to the complete system at a sampling rate (f_s) of 44,1 kHz.
- Value relative to 1 V_(rms), with unity gain.
- Unity gain output = 1 V_(rms).
- Minimum V_{IL}, V_{OL} and maximum V_{IH}, V_{OH} are peak values to allow for transients.
- I_{LI}(min) and I_{LO}(min) measured at V_I = 0 V; I_{LI}(max) and I_{LO}(max) measured at V_I = V_{DD}.
- Reference levels = 0,8 V and 2,0 V.
- Output times are measured with a capacitive load of 35 pF.
- t_{HIGH} valid only when used with XTAL.

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(a)

Fig. 4(a) Typical I²S data input waveforms at 2,8 MHz.



(b)

Fig. 4(b) Typical I²S data output waveforms at 5,6 MHz.

TIMING

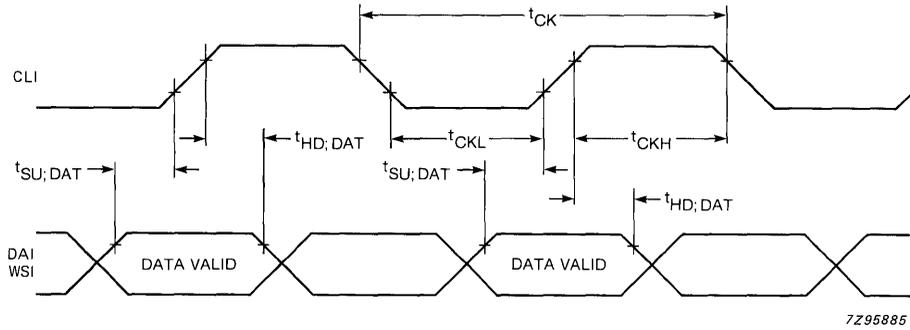
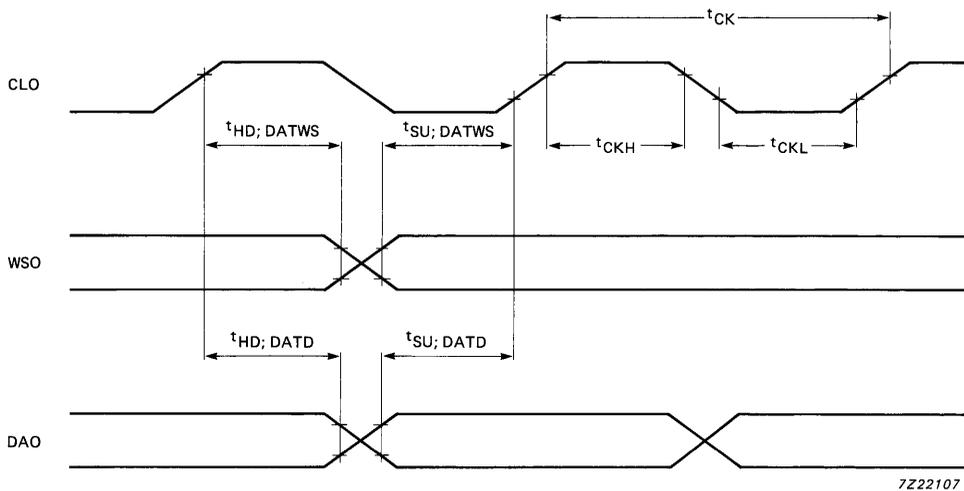


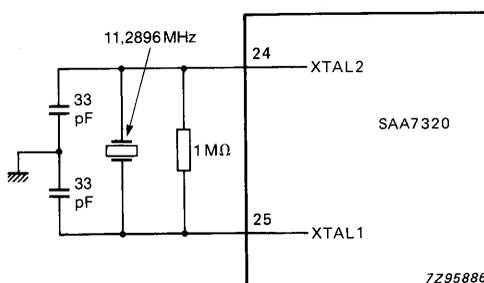
Fig. 5 Data input timing with respect to I²S serial bit clock input (CLI);
reference levels = 0,8 V and 2,0 V.

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7Z22107

Fig. 6 Data output timing with respect to clock output (CLO); reference levels = 0,8 V and 2,0 V.



7Z95886

Fig. 7 Crystal oscillator circuit using crystal type: 4322 143 05031.

APPLICATION INFORMATION

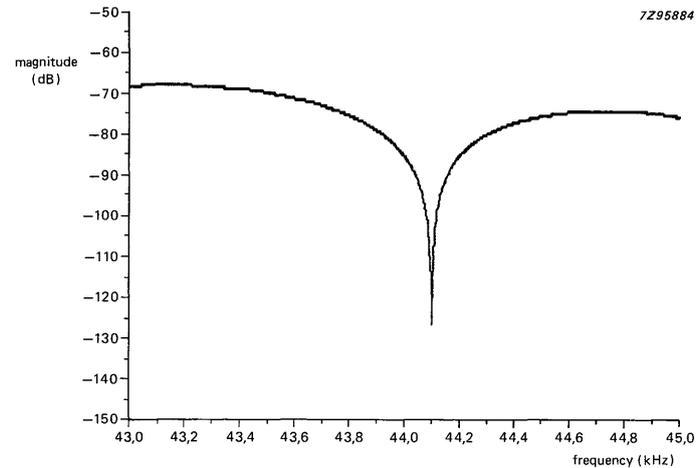
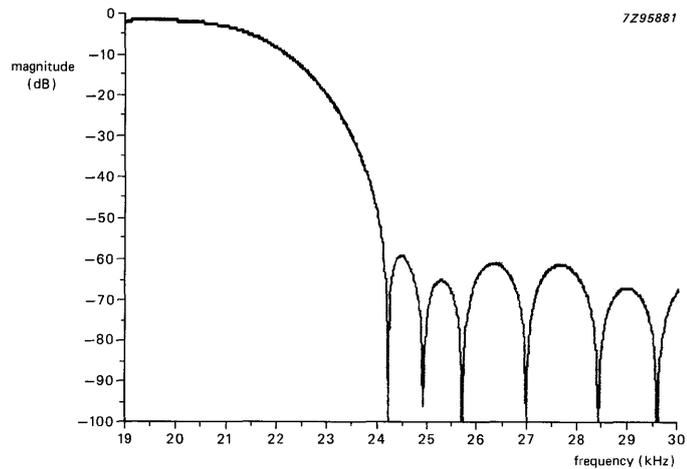
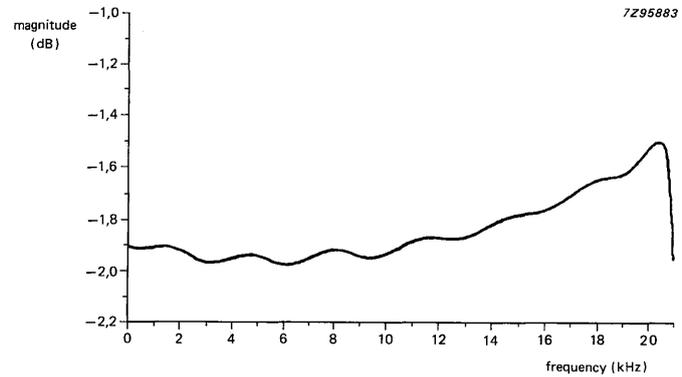
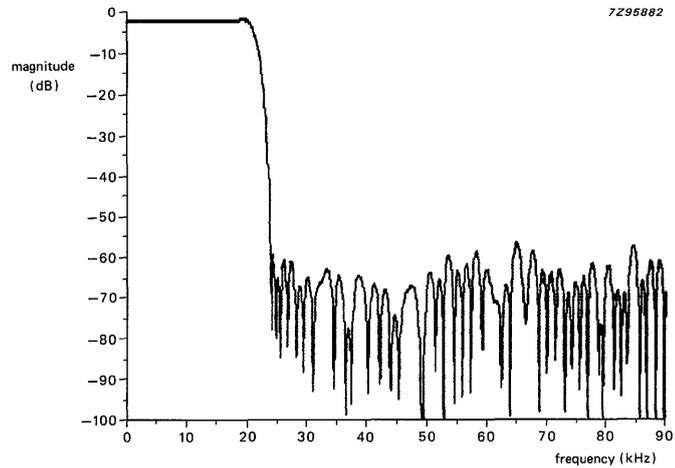
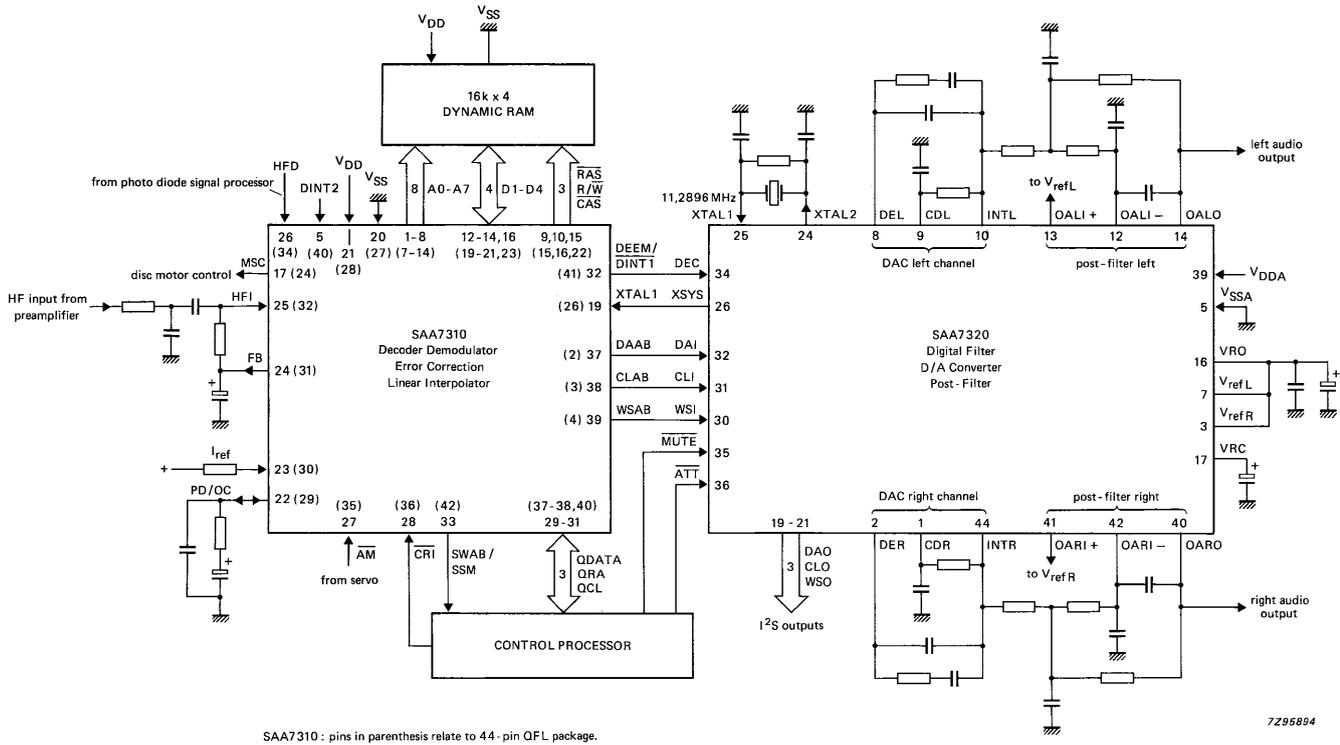


Fig. 8 Digital filter characteristics; magnitude as a function of frequency.

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SAA7310 : pins in parenthesis relate to 44 - pin QFL package.

Fig. 9 System application diagram; CD3A with the DAC3.

Stereo CMOS DAC for compact disc digital audio systems

SAA7320